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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,883	08/20/2003	Masashi Shima	031027	5221
38834	7590	10/25/2004	EXAMINER	
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036			QUINTO, KEVIN V	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 10/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/643,883

Applicant(s)

SHIMA, MASASHI

Examiner

Kevin Quinto

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2826

mw

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 October 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 11-21 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5-9 is/are allowed.
- 6) ☒ Claim(s) 1-4 and 10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-10 in the reply filed on September 30, 2004 is acknowledged.
2. Claims 11-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on September 30, 2004.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
5. Claims 1-4 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
6. Claim 1 recites the limitation "the active layer" in lines 7-8. There is insufficient antecedent basis for this limitation in the claim.

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7. The examiner believes that the intended term is "the active region" and has thus interpreted the claim in this manner.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by

Ichinose et al. (United States Patent Application No. US 2004/0009636 A1).

10. So far as understood in claim 1, Ichinose et al. (United States Patent Application No. US 2004/0009636 A1, hereinafter referred to as the "Ichinose" reference) discloses a similar device. Figure 13 of Ichinose discloses a semiconductor device with a SiGe layer (1b) formed on a silicon substrate (1a). An element isolation groove is formed in the surface of the SiGe layer (1b) thus defining an active region. A silicon layer (3) is formed on the sidewall of the element isolation groove and the SiGe layer (1b) in the active region. An element isolation insulation film (7) is buried in the element isolation groove with the silicon layer (3).

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11. Claims 1, 2, 4, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohnishi et al. (United States Patent Application No. US 2004/0121554 A1).

12. So far as understood in claim 1, Ohnishi et al. (United States Patent Application No. US 2004/0121554 A1, hereinafter referred to as the "Ohnishi" reference) discloses a similar device. Figures 1-8 of Ohnishi disclose a semiconductor device with a SiGe layer (12) formed on a silicon substrate (11). An element isolation groove is formed in the surface of the SiGe layer (12) thus defining an active region (31). A silicon layer (13) is formed on the sidewall of the element isolation groove and the SiGe layer (12) in the active region (31). An element isolation insulation film (14 or 15 or 16) is buried in the element isolation groove with the silicon layer (13).

13. So far as understood in claim 2, a source layer (65) and a drain layer (65) are formed in the active region (31). A gate electrode (63) is formed on the silicon layer (13) between the source layer (65) and the drain layer (65) with a gate insulation film (62) formed between the silicon layer (13) and the gate electrode (63). The examiner notes the "diffused layer" limitation with regard to the source and drain layers. However this limitation places claim 2 into the form of a **product-by-process claim**:

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Thorpe*, 227 USPQ 964, 966; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claim 2 does not distinguish over the Ohnishi reference regardless of the process used to form the source and the drain layers, because only the final product is relevant, and not the process of making such as diffusion.

14. So far as understood in claim 4, an insulation film (14 or 15 or 16) is formed on the silicon layer (13) on the sidewall of the element isolation groove.

15. So far as understood in claim 10, an insulation film (15) is a silicon nitride film (p.3, paragraph 59).

16. So far as understood in claim 1, Ohnishi (US 2004/0121554 A1) discloses a similar device. Figures 9-15 of Ohnishi disclose a semiconductor device with a SiGe layer (12) formed on a silicon substrate (11). An element isolation groove is formed in the surface of the SiGe layer (12) thus defining an active region. A silicon layer (81, 101) is formed on the sidewall of the element isolation groove and the SiGe layer (12) in the active region. An element isolation insulation film (102 or 111) is buried in the element isolation groove with the silicon layer (101).

17. So far as understood in claim 2, a source layer (65) and a drain layer (65) are formed in the active region. A gate electrode (63) is formed on the silicon layer (81) between the source layer (65) and the drain layer (65) with a gate insulation film (62) formed between the silicon layer (81) and the gate electrode (63). The examiner notes the "diffused layer" limitation with regard to the source and drain layers. However this limitation places claim 2 into the form of a

product-by-process claim:

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Thorpe*, 227 USPQ 964, 966; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and

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In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claim 2 does not distinguish over the Ohnishi reference regardless of the process used to form the source and the drain layers, because only the final product is relevant, and not the process of making such as diffusion.

18. So far as understood in claim 4, an insulation film (102 or 111) is formed on the silicon layer (101) on the sidewall of the element isolation groove.

19. So far as understood in claim 1, Ohnishi (US 2004/0121554 A1) discloses a similar device. Figures 16-21 of Ohnishi disclose a semiconductor device with a SiGe layer (12) formed on a silicon substrate (11). An element isolation groove is formed in the surface of the SiGe layer (12) thus defining an active region. A silicon layer (81, 171a) is formed on the sidewall of the element isolation groove and the SiGe layer (12) in the active region. An element isolation insulation film (172 or 181) is buried in the element isolation groove with the silicon layer (171a).

20. So far as understood in claim 2, a source layer (65) and a drain layer (65) are formed in the active region. A gate electrode (63) is formed on the silicon layer (81) between the source layer (65) and the drain layer (65) with a gate insulation film (62) formed between the silicon layer (81) and the gate electrode (63). The examiner notes the "diffused layer" limitation with regard to the source and drain layers. However this limitation places claim 2 into the form of a **product-by-process claim:**

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Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Thorpe*, 227 USPQ 964, 966; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claim 2 does not distinguish over the Ohnishi reference regardless of the process used to form the source and the drain layers, because only the final product is relevant, and not the process of making such as diffusion.

21. So far as understood in claim 4, an insulation film (172 or 181) is formed on the silicon layer (171a) on the sidewall of the element isolation groove.

22. So far as understood in claim 1, Ohnishi (US 2004/0121554 A1) discloses a similar device. Figures 22-29 of Ohnishi disclose a semiconductor device with a SiGe layer (12) formed on a silicon substrate (11). An element isolation groove is formed in the surface of the SiGe layer (12) thus defining an active region. A silicon layer (81, 261) is formed on the sidewall of the element isolation groove and the SiGe layer (12) in the active region. An element isolation insulation film (271 or 281) is buried in the element isolation groove with the silicon layer (261).

23. So far as understood in claim 2, a source layer (65) and a drain layer (65) are formed in the active region. A gate electrode (63) is formed on the silicon layer (81) between the source layer (65) and the drain layer (65) with a gate insulation film (62) formed between the silicon layer (81) and the gate electrode (63). The examiner notes the "diffused layer" limitation with regard to the source and drain layers. However this limitation places claim 2 into the form of a

product-by-process claim:

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Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Thorpe*, 227 USPQ 964, 966; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claim 2 does not distinguish over the Ohnishi reference regardless of the process used to form the source and the drain layers, because only the final product is relevant, and not the process of making such as diffusion.

24. So far as understood in claim 4, an insulation film (271 or 281) is formed on the silicon layer (261) on the sidewall of the element isolation groove.

Allowable Subject Matter

25. Claims 5-9 are allowed.

26. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a semiconductor device with collector and base regions formed in a semiconductor substrate which are separated by trench isolation regions that have Si and SiGe layers formed within them.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ



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